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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,408	04/19/2004	Viswanathan Lakshmanan	03-2644 81693	4517

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EXAMINER	
PARIHAR, SUCHIN	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,408	LAKSHMANAN ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This application 10/828,408 has been examined. Claims 1-10 are pending.

Specification

1. The abstract of the disclosure is objected to because it lacks narrative format. The abstract should be a narrative description of the invention. Correction is required. See MPEP § 608.01(b).

2. The disclosure is objected to because of the following informalities: the section titled "Summary of the Invention" is objected to for merely reciting the independent claims 1 and 5. Appropriate correction is required. See MPEP § 608.01(d).

Claim Objections

3. Claim 1 is objected to because of the following informalities: The phrase "streaming out", found on the last line of both claims 1 and 5, lacks clarity in light of the specification. Appropriate correction is required.

4. Claims 3 and 8 are objected to because of the following informalities: The phrase, "the marked integrated circuit design database", beginning on line 2 of claim 3, lacks antecedent basis. Claim 8 follows similarly. Examiner interprets "the marked integrated circuit design database" as the same database discussed in steps c) and f) of both claims 1 and 6. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1 and 6 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Morgan (6,530,073) in view of Tester (6,922,823).

7. With respect to claims 1 and 6, Morgan teaches a method and computer program product (Col 5, lines 38-55, i.e. discussion of computer languages and systems) of verifying an incremental change to an integrated circuit design comprising steps of: (a) receiving as input an integrated circuit design database (see Fig 1A, i.e. Original RTL netlist as input); (b) receiving as input an engineering change order (Col 6, lines 5-18, i.e. ECO changes made by the user [input]); (c) identifying and marking objects in the integrated circuit design database to indicate a current state of the integrated circuit design database (Col 6, lines 52-62, i.e. using original RTL netlist to generate a list of logic gates and their interconnections of the original circuit [the current state]); (d) applying the engineering change order to the integrated circuit design database (Col 10, lines 5-15, i.e. ECO changes are made to a circuit); (e) analyzing the integrated circuit design database to generate a list of incremental changes to the integrated circuit design database resulting from the engineering change order (Col 11, lines 40-50, i.e. ECO changes lead to a list of changes, [for incremental changes, see lines 35-40]); and (f) identifying and marking objects in the integrated circuit design database included in the list of incremental changes to distinguish objects in the integrated circuit design database that were changed from the current state (Col 11, lines 40-50, i.e. comparison between ECO gate-level netlist and original netlist, which as a result generates the list

of changes). Morgan does not teach: (g) streaming out the integrated circuit design database. However, Tester (6,922,823) teaches a method of making changes to existing layouts and/or creating new layouts for related products wherein the following is performed as the last step in the process of Figure 1: (g) streaming out the integrated circuit design database (see Figure 1, #38, streaming out GDSII layout file for release to the foundry; also see Col 2, lines 10-15). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Tester into the invention of Morgan because the streaming out of a GSDII layout file improves the invention of Morgan by providing a means for mask and/or device manufacturing at the end of a design process.

8. **Claims 2-5 and 7-10 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Morgan (6,530,073) in view of Tester (6,922,823), and in further view of Sung et al. (US PG Pub 2005/0216872).

9. With respect to claims 2 and 7, Morgan in view of Tester teaches all the elements of claims 1 and 6, from which the claims depend respectively. Morgan in view of Tester does not teach: wherein step (g) [of claims 1 and 6] comprises translating the integrated circuit design database to a file in generic data stream format. However, Sung teaches: wherein step (g) [of claims 1 and 6] comprises translating the integrated circuit design database to a file in generic data stream format (pg 4, paragraph [0044], i.e. discussion of gate-level netlist [IC design database] going through a placement and routing step, and then being output as a GDS format data file; also see Fig 5). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Sung

into the invention of Morgan and Tester because Sung would improve the method of Morgan by enabling a physical view of an IC [GDS format file] to be verified against a gate-level netlist [original IC database]. Note that applicant also suggests the use of a GDS format file for use in an IC verification process (see applicant's specification, pg 7, lines 20-29).

10. With respect to claims 3 and 8, Morgan in view of Sung teaches all the elements of claims 2 and 7, from which the claims 3 and 8 depend, respectively. Morgan teaches: applying a special rule deck to validate the marked integrated circuit design database wherein the special rule deck includes only design checks and rules applicable to the objects that were changed from the current state (Col 9, lines 32-51, i.e. annotated constraint file H [special rule deck] to validate netlist output E, wherein constraints [rules] in constraint file H reflect and comport to the changes made in the new RTL netlist of output G).

11. With respect to claims 4 and 9, Morgan in view of Sung teaches all the elements of claims 3 and 8, from which the claims 4 and 9 depend, respectively. Morgan teaches: step of identifying a design rule violation in the objects that were changed from the current state (see Fig 1B, i.e. annotated design 270 receives timing verification [or other design rule verification, see Col 10, lines 45-50] and decision box 310 determines design rule violation).

12. With respect to claims 5 and 10, Morgan in view of Sung teaches all the elements of claims 4 and 9, from which the claims 4 and 9 depend, respectively. Morgan teaches: step of modifying the integrated circuit design database to correct the

design rule violation (see Fig 1A, i.e. #90, fix invalid constraints of the IC design database).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suchin Parihar
Examiner
AU 2825

STACY A. WHITMORE
PRIMARY EXAMINER